EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Stankiewicz (RN: 60,169) and Amy Bizon-Copp (RN 53,993) on April 08, 2009.

The application has been amended as follows:

IN THE TITLE

THIN FILM TRANSISTOR ARRAY PANEL ~~AND METHOD MNUFACTURING THE SAME~~

IN THE CLAIMS

1. (Currently Amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire from a plurality of gate wires formed on the insulating substrate, the gate wire ~~and~~ including a plurality of gate line portions and a gate connection connecting the gate line portions;

a data wire from a plurality data wires insulated from the gate wires and intersecting the gate wires, the data wire comprising a plurality of data line portions and a data connection connecting the data line portions;

a gate insulating layer insulating the gate wire and the data wire, ~~and including a plurality of portions, and~~ a portion of the gate insulating layer ~~is~~ being disposed between the plurality of gate ~~line~~ portions and the gate connection;

a thin film transistor ~~formed by~~ including a gate electrode ~~a portion of~~, of the gate wire and ~~a portion of~~ source electrode connected to the data wire; and

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a pixel electrode connected to a drain electrode of the thin film transistor,

wherein the gate electrode, the gate line portions and the data connection are formed from a same first layer; and the gate connection, the source electrode, the drain electrode and the data line portions are formed from a same second layer;

wherein at least a portion of the gate insulating layer is formed on the first layer; and

wherein the gate connection is formed between two of the plurality of data wires; and the data connection is formed between two of the plurality of gate wires .

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The thin film transistor array panel of claim 1, further comprising a passivation layer covering the thin film transistor~~s and including a plurality of portions~~.

5. (Currently Amended) The thin film transistor array panel of claim ~~2~~ 1,wherein the gate connection is ~~disposed on the same layer as the data line portions, and~~ connected to the gate ~~line~~ portions through first contact holes provided ~~at~~ in the gate insulating layer.

6. (Currently Amended) The thin film transistor array panel of claim ~~2~~ 1, wherein the data connection is ~~disposed on the same layer as the gate line portions, and~~

connected to the data line portions through second contact holes provided ~~at~~ in the gate insulating layer.

7. (Currently Amended) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire from a plurality of gate wires, the gate wire being formed on the insulating substrate, and including first and second gate line portions and a gate connection connecting the first and second gate line portions;

a gate insulating layer formed on a portion of the gate wire, and including first and second contact holes;

a semiconductor layer formed on a predetermined area of the gate insulating layer;

an ohmic contact layer formed on the semiconductor layer and having a shape substantially the same as the semiconductor layer except for a predetermined area of the semiconductor layer;

a data wire from a plurality of data wires insulated from the gate wires and intersecting the gate wires, the data wire including first and second data line portions, and the data wire is connected to a source electrode overlapping the ohmic contact layer at least in part;

a passivation layer formed on the data wire and having a third contact hole exposing a drain electrode ~~the data wire~~;

a pixel electrode formed on the passivation layer and connected to the ~~data wire~~ drain electrode through the third contact hole,

~~wherein the first and second gate line portions, and a portion of the gate wire is formed on the same layer as a portion of the data wire,~~

wherein a portion of the gate insulating layer is disposed between the first gate line portion and the gate connection, and between the second gate ~~wire portion~~ line portion and the gate connection; ~~, and~~

wherein the first and the second gate line portions are connected to the gate connection through the first contact hole;

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wherein a gate electrode, the first and second gate line portions and the data connection are formed from a same first layer; and the gate connection, the source electrode, the drain electrode and the first and second data line portions are formed from a same second layer; and

wherein the gate connection is formed between two of the plurality of data wires; and the data connection is formed between two of the plurality of gate wires .

8. (Currently Amended) The thin film transistor array panel of claim 7, wherein the data wire includes first and second data ~~line~~ portions, and a data connection formed on the same layer as the portion of the gate wire, and the first and the second data line portions are connected to the data connection through the second contact hole.

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9. (Currently Amended) The thin film transistor array panel of claim 7, wherein the first and the second gate ~~line~~ portion each comprise a gate line extending in a direction and a gate electrode, which is a portion of the gate line, and the first gate line portion further comprises a gate pad provided at an end of the respective gate wire ~~line~~.

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10. (Currently Amneded) The thin film transistor array panel of claim 7, wherein the gate wire and the data wire intersect to define a pixel area, and portions of at least one of the gate insulating layer and the passivation layer near ~~in~~ the pixel electrode ~~is~~ are removed.

11. (Currently Amended) The thin film transistor array panel of claim 8, wherein the first and the second data ~~line~~ portion each comprise a data line extending in a direction, a source electrode, which is a portion of the data line and overlaps the ohmic contact layer in part, and a drain electrode located opposite the source electrode and overlapping the ohmic contact layer in part, and the first data line portion further comprises a data pad provided at an end of the data wire ~~line~~.

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12. (Original) The thin film transistor array panel of claim 10, wherein at least one of the gate insulating layer and the passivation layer is divided into a plurality of portions by an opening extending parallel to the gate wire, and the opening is located between adjacent gate ~~lines~~ wires and connected to ~~the~~ a predetermined area of the pixel area.

13-15. (Currently Cancelled).

Allowable Subject Matter

Claims 1 and 4-12 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference A is cited as being related to a TFT display device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811